UNITED STATES PATENT APPLICATION

FOR

FORWARD ERROR CORRECTION MAPPING AND DE-MAPPING TECHNIQUES

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FORWARD ERROR CORRECTION MAPPING AND DE-MAPPING TECHNIQUES

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Cross Reference to Related Patent Application

[0001]   The present application is related to U.S. Patent Application No. 10/113,190, filed

April 1, 2002, inventors Poppinga and Kauschke (Attorney Docket No. P12259).

Field

[0002]   The subject matter disclosed herein generally relates to forward error correction

mapping techniques.

Description of Related Art

[0003]   ITU-T G.709/Y.1331 Interfaces for the Optical Transport Network (OTN) (Feb.

2001) describes a convention for conversion of signals between the optical transport network

(OTN) standard and either Synchronous Optical Network (SONET) or Synchronous Digital

Hierarchy (SDH) standards. G.709 describes forward error correction (FEC) as a manner of

controlling errors in transmitted data. FEC information is transmitted with data and can be used

by the receiver to check and correct the data. G.709 describes Reed-Solomon coder/decoder

techniques for determining and mapping FEC information into designated locations within an

OTN frame as well as techniques for processing and de-mapping FEC information.

Brief Description of the Drawings

[0004]   The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

[0005]   FIG. 1A depicts an implementation of a transmitter system that can use embodiments of the present invention;

[0006]   FIG. 1B depicts an implementation of a receiver system that can use embodiments of the present invention;

[0007]   FIGs. 2A to 2E depict frames of varying formats in accordance with an embodiment of the present invention;

[0008]   FIG. 3 depicts an encoder, in accordance with an embodiment of the present invention;

[0009]   FIGs. 4A and 4B depict example frame streamings; and

[0010]   FIG. 5 depicts an embodiment of a decoder, in accordance with an embodiment of the present invention.

[0011]   Note that use of the same reference numbers in different figures indicates the same or like elements.

Detailed Description

[0012]   FIG. 1A depicts an implementation of a transmitter system 10 that can use

embodiments of the present invention. System 10 may include a network 11, client signal

processor 12, wrapper system 13, output system 14, and bus 15.

[0013]   Network 11 may provide intercommunication between processor 12 and other

devices such as a packet processor (not depicted), and/or a switch fabric (not depicted).

Network 11 may comply with one or more of the following standards: Ten Gigabit Attachment

Unit Interface (XAUI) (described in IEEE 802.3, IEEE 802.3ae, and related standards), (Serial

Peripheral Interface (SPI), I^2C, universal serial bus (USB), IEEE 1394, Gigabit Media

Independent Interface (GMII) (described in IEEE 802.3, IEEE 802.3ae, and related standards),

Peripheral Component Interconnect (PCI), ten bit interface (TBI), and/or a vendor specific multi-

source agreement (MSA) protocol.. Bus 15 may provide intercommunication between client

signal processor 12, and/or wrapper system 13, and/or output system 14 and other devices such

as memory device (not depicted), or microprocessor (not depicted).

[0014]   Processor 12 may perform media access control (MAC) encoding in compliance

for example with Ethernet (as described for example in IEEE 802.3 and related standards).

Wrapper system 13 may perform framing and wrapping in compliance for example with ITU-T

G.709; and/or forward error correction (FEC) encoding in compliance for example with ITU-T

G.975. Wrapper system 13 may use some embodiments of the present invention. Output system

14 may remove jitter from signals provided by wrapper system 13 and prepare signals for

transmission to a network 16, which may be optical or electrical format. For example, network

16 may comply with OTN.

[0015]   In one implementation, components of transmitter system 10 may be implemented among the same integrated circuit. In another implementation, components of transmitter system 10 may be implemented among several integrated circuits that intercommunicate using, for example, a bus or conductive leads of a printed circuit board.

[0016]   FIG. 1B depicts an implementation of a receiver system 20 that can use embodiments of the present invention. System 20 may include an input system 22, de-wrapper system 23, client signal processor 24, network 26, and bus 27. Input system 22 may receive a signal from a network 21 and prepare the signal for processing by receiver system 20. For example, input system 22 may convert an optical signal to electrical format and/or remove jitter from a signal from the network. De-wrapper system 23 may perform optical transport network (OTN) de-framing and de-wrapping in compliance for example with ITU-T G.709; and/or forward error correction (FEC) processing in compliance for example with ITU-T G.975. De-wrapper system 23 may use some embodiments of the present invention. Processor 24 may perform media access control (MAC) processing in compliance for example with Ethernet.

[0017]   Network 26 may provide intercommunication between processor 24 and other devices such as a packet processor (not depicted), a switch fabric (not depicted), and/or an optical network (not depicted). Network 26 may utilize similar communications techniques as those of network 11. Bus 27 may provide intercommunication between input system 22 and/or de-wrapper 23 and/or processor 24 and other devices such as a memory device (not depicted) or microprocessor (not depicted).

[0018]   In one implementation, components of receiver system 20 may be implemented among the same integrated circuit. In another implementation, components of receiver system

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20 may be implemented among several integrated circuits that intercommunicate using, for example, a bus or conductive leads of a printed circuit board.

[0019]   FIGs. 2A to 2E depict frames of respective formats 400, 500, 501, 502, and 401. Frame format 400 may comply with the G.709 OTU2 frame format, although other formats may be used. Frame format 400 may include management overhead, client data, and error correction portions. Frame format 400 may have fixed length and a fixed number of rows. In one example, the client data portion may include data in accordance with the SONET or OTN standards.

[0020]   Frame format 500 may include a first portion that includes a mixture of client data (from frame format 400), G.709 overhead information (from frame format 400), and reserved space for column parity information as well as a second portion reserved for row parity information. The reserved space for column parity information may be diagonally provided within the first portion. Frame format 500 may be configurable in the following parameters: number of columns, number of rows, the angle and thickness of the column parity information provided within the first portion, and size of row parity information. The parameters may be set to maintain the percentage of bits reserved for client data (from frame format 400) and G.709 overhead information (from frame format 400) among frame format 400 as the same percentage as that in frame format 500.

[0021]   In one implementation, depicted in FIG. 4A, frames of format 500 might stream in a concatenation style as continuous series of separate frames. In this concatenation style, there might be no time gap between two successive frames of format 500. Format 500 may also be processed using an interleaving style such as one described in U.S. Patent Application No. 10/113,190, filed April 1, 2002, inventors Poppinga and Kauschke. As depicted in FIG. 4B,

the interleaving style may include streaming frames of format 500 as a continuous series of

separate frames except column parity information of a single frame of format 500 is spread over

multiple frames of format 500. Herein, references to "format 500" or "frame format 500" may

refer to streaming in either the concatenation or interleaving styles.

[0022]   Frame format 501 may be a similar structure as frame format 500 but with column

parity information inserted in the reserved space for column parity information. Frame format

502 may be a similar structure as frame format 501 but with row parity information inserted in

the reserved space for row parity information. Similar to format 500, formats 501 and 502 may

stream by concatenation or interleaving styles.

[0023]   Frame format 401 may be similar to frame format 400 except at least that the

error correction portion may include column and row parity information and synchronization

information. For example, column and row parity information may be stored in a similar order

as that stored in a frame of format 502. Synchronization information may indicate locations of

column and row parity information within frame format 502. Synchronization information may

be stored within a predefined location within the error correction portion of frame format 401. In

one implementation, synchronization information could be defined in each frame of format 401,

but could also appear in every N frames of format 401, where N is an integer greater than one.

Alternatively, the synchronization information may be partitioned in a way that every frame one

fraction of the synchronization information will be transmitted so that it may take an integer N

number of frames of format 401 (where N is greater than one) to transmit the entire

synchronization information of a single frame of format 401. Management overhead and client

data may be mapped into locations in frame 401 that are similar to those locations in frame 400.

[0024]   FIG. 3 depicts an embodiment of the present invention in an encoder 600, in accordance with an embodiment of the present invention. One implementation of encoder 600 may include synchronizer 602, first mapper 604, column encoder 606, row encoder 608, and second mapper 610. Reference is made to frames having formats 400, 500, 501, 502, and 401 depicted in respective FIGs. 2A to 2E.

[0025]   Encoder 600 may be implemented as any or a combination of: hardwired logic, software stored by a memory device and executed by a microprocessor, firmware, an application specific integrated circuit (ASIC), and/or a field programmable gate array (FPGA).

[0026]   Synchronizer 602 may track the bit locations of column and row parity information within a frame of format 500. Synchronizer 602 may provide the bit locations of column and row parity information to column encoder 606, row encoder 608, and second mapper 610. Synchronizer 602 may store synchronization information within a frame of format 401. The synchronization information may represent the timing and phase locations of column and row parity information within a frame of format 500.

[0027]   First mapper 604 may convert a frame from format 400 to format 500. First mapper 604 may reserve space for column parity information as well as space for row parity information. In the locations inside format 500 depicted as "client data & OH", first mapper 604 may insert client data and management overhead. First mapper 604 may initialize the bits reserved for column and row parity information to zeros. In one implementation, encoder 600 may vary parameters of a frame of format 500 based on the desired level of FEC protection.

[0028]   Column encoder 606 may insert column parity information into space reserved for column parity information in a frame of format 500. Row encoder 608 may insert row parity

information into space reserved for row parity information in a frame of format 500. For example, Bose, Chaudhuri and Hocquenghem (BCH) or Reed Solomon (RS) encoding techniques may be used to determine column and row parity information stored in frame format 500. Calculation of column and row parity information may be based on processing client data. Calculation of column and row parity information may also be based on parameters such as overhead values and parameters of frame format 502 that include, but are not limited to, a number of columns, number of rows, the angle and thickness of the column parity information, and size of row parity information.

[0029]   Second mapper 610 may convert a frame from format 502 to format 401. Second mapper 610 may map the client data and management overhead into locations inside the frame of format 401 that are similar to those of format 400 and may map column and row parity information as well as synchronization information into the error correction portion of a frame of format 401. A frame of format 401 may be transmitted to a network such as an optical network or electrical network.

[0030]   Encoder 600 may provide stronger FEC encoding protection than that specified in G.709. Accordingly, by use of encoder 600, signals can be transmitted over systems that introduce higher bit errors. Encoder 600 may provide stronger FEC protection than that specified in G.709 without changing a line rate of management overhead and client data or the transmitted frame structure.

[0031]   FIG. 5 depicts an embodiment of the present invention in decoder 700, in accordance with an embodiment of the present invention. One implementation of decoder 700 may include synchronization information extractor 702, third mapper 704, column and row

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decoder stages 706, and fourth mapper 708. Reference is made to frames having formats 400, 500, 501, 502, and 401 depicted in respective FIGs. 2A to 2E. For example, decoder 700 may process a frame of format 401 transmitted through a network and from a transmitter using an encoder similar to encoder 600.

[0032]   Decoder 700 may be implemented as any or a combination of: hardwired logic, software stored by a memory device and executed by a microprocessor, firmware, an application specific integrated circuit (ASIC), and/or a field programmable gate array (FPGA).

[0033]   Synchronization information extractor 702 may extract synchronization information from a frame of format 401. Synchronization information extractor 702 may provide the locations of column and row parity information in a frame of format 502.

[0034]   Third mapper 704 may convert a frame from format 401 to format 502. For example, third mapper 704 may read the column and row parity information that is stored in an error correction portion of a frame of format 401. For example, third mapper 704 may store the column and row parity information in locations in a frame of format 502 indicated by the synchronization information.

[0035]   Column and row decoder stages 706 may decode column and row bit information stored in a frame of format 502. For example in one implementation, column and row decoder stages 706 may utilize BCH or RS techniques to process the column and row bit information and determine whether such processed column and row bit information are correct. Based on the processed column and row bit information, column and row decoder stages 706 may perform error detection and/or correction of management overhead, client data and parity information. Column and row decoder stages 706 may also calculate error statistics in the frames of format

500. For example, error statistics may relate to the percentage of the bandwidth utilized by a frame of format 500. For example, error statistics may relate to management overhead and client data.

[0036]   In one implementation, column and row decoder stages 706 may perform iterative decoding by alternating processing of rows and columns and performing at least two row or column processings. For example, column and row decoder stages 706 may alternate processing of all rows of a frame of format 502, all columns of a frame of format 502, and (again) all rows of a frame of format 502 or processing of all columns, all rows, and (again) all columns. In one implementation, column and row decoder stages 706 may perform bit processing in the following manner: all rows of a frame of format 502, all columns of a frame of format 502, (again) all rows, (again) all columns, and (again) all rows. In one implementation, column and row decoder stages 706 may perform concatenated decoding by bit processing all rows and all columns once each.

[0037]   Fourth mapper 708 may convert a frame from format 502 to format 400 or format 401. Fourth mapper 708 may map the client data and management overhead into its original locations inside the frame of format 400 or 401. Fourth mapper 708 may use techniques similar to those described with respect to second mapper 610 to convert a frame of format 502 to format 401.

Modifications

[0038]   The drawings and the forgoing description gave examples of the present

invention. The scope of the present invention, however, is by no means limited by these specific

examples. Numerous variations, whether explicitly given in the specification or not, such as

differences in structure, dimension, and use of material, are possible. The scope of the invention

is at least as broad as given by the following claims.